

CompactPCI[®] PlusIO

Short Form Specification



**Open Modular
Computing Specifications**

NOTE: This short form specification is a subset of Revision 1.0 of the CompactPCI PlusIO specification PICMG 2.30. For complete guidelines on the design of CompactPCI PlusIO compliant boards and systems, the full specification is required.

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1 General

1.1 Overview

CompactPCI® PlusIO defines the usage of rear I/O pins of the 32-bit CompactPCI® system slots for high-speed serial signals. This allows interoperability with all other CompactPCI® 2.xx standards by PICMG for 3U as well as for 6U cards which do not use these pins.

For these high-speed signals a new J2 connector is introduced which is designed to be intermateable to backplanes defined in the CompactPCI® base specification. This connector is able to support differential signals up to 5 Gb/s.

This means system slot boards with this new high-speed connector can be used in existing 32-bit systems. The J2 pin assignment also interoperates with 64-bit backplanes provided the peripheral boards do not connect to 64-bit signals; of course the serial I/O cannot be used in that case.

The main advantage of the combination of legacy PCI and modern serial buses on J2/P2 is to realize hybrid backplanes. This standard helps to define a simple migration path from parallel PCI systems to modern serial, point-to-point interconnected systems like CompactPCI® Serial.

The specification defines the support of PCI, PCI Express, Ethernet, SATA/SAS and USB concurrently. In addition to the parallel PCI bus architecture it allows the use of the CompactPCI® system slot to provide a simple star architecture based on the specified serial bus standards.

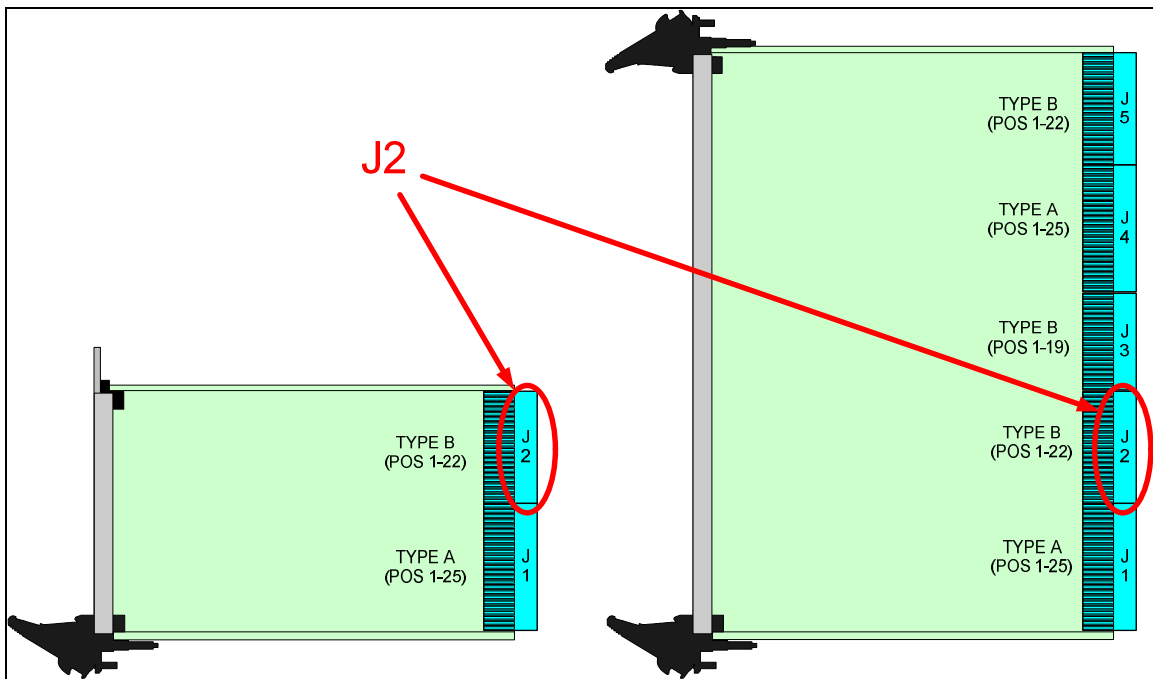


Figure 1. J2 Identification

Extending CompactPCI by CompactPCI PlusIO

The original CompactPCI® architecture is based on a parallel bus which connects the system slot to the peripheral slots. PICMG 2.16 – a CompactPCI extension – introduced Ethernet on the backplane as another transmission medium beside the parallel PCI bus. CompactPCI Express turns away completely from the parallel PCI bus and is based exclusively on PCI Express® as a fast serial point-to-point connection.

To improve the bandwidth, chipsets have been extended by serial high-speed interfaces. These point-to-point connections are optimized depending on the connected devices. For closely coupled extensions, PCI Express was introduced to replace the parallel PCI bus. For hard drives, SATA or SAS were established. Slower, not so closely coupled devices are connected by USB.

The new standard PICMG 2.30 CompactPCI® PlusIO extends CompactPCI® by PCI Express® and Ethernet for multiprocessing, SATA/SAS for building RAID hard disk systems and USB for connecting radio modules (wireless communication like WiFi etc.). The parallel PCI bus will stay for existing I/O, but is limited to 32 bits.

CompactPCI® PlusIO uses the user I/O pins of the system slot in order to support legacy PCI slots as well as slots based on modern serial interconnects. No bridges or switches are required for this. For multiprocessing applications, Ethernet is the most common solution to connect CPUs.

PICMG 2.30 defines just the system slot extension. For peripheral boards – depending on the interface – CompactPCI® Serial, CompactPCI® Express or PICMG 2.16 boards can be combined.

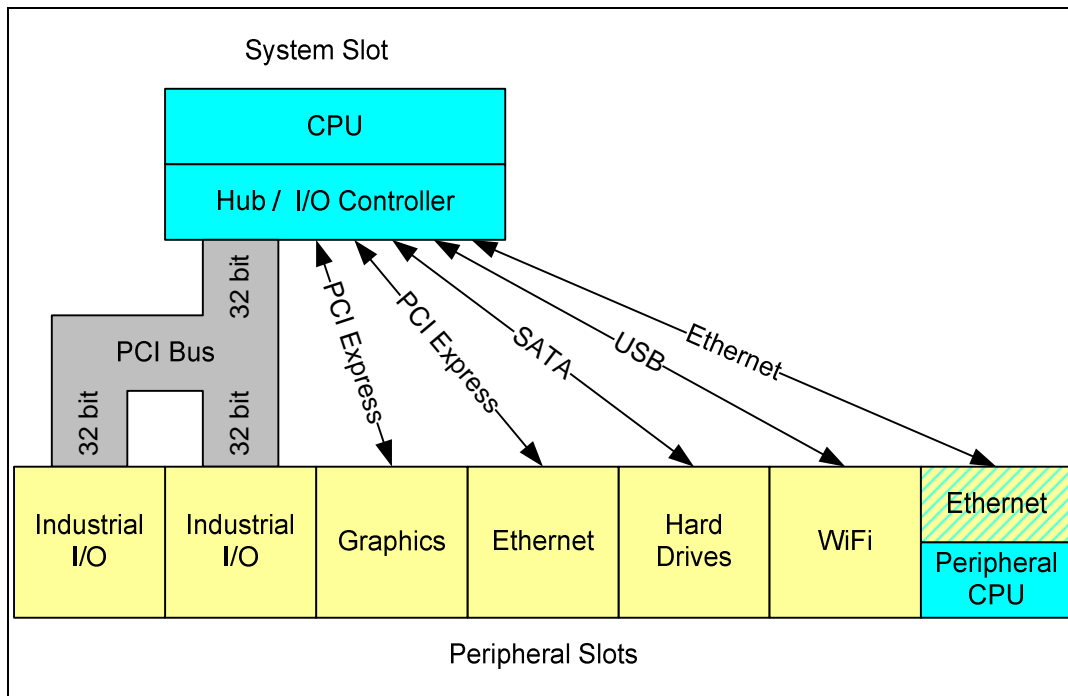


Figure 2. Architectural Extensions by Serial Busses

1.2 Interoperability

The CompactPCI PlusIO specification defines the user-defined pins of the 32-bit system slot definition in a way to bring out the serial interconnections on J2 to the backplane. This definition does not violate the existing standard so that the two are fully interoperable. The standard J2 (2-mm HM) connector is not able to support differential signals up to PCI Express generation 2 (5 Gb/s). So the connector used for J2 had to be improved as well. Such connectors, which are designed to be compatible to the IEC specification, are available on the market and are used on system slots compliant to CompactPCI PlusIO. The backplane connector does not have to be modified.

In addition a hybrid backplane can be realized by combining a CompactPCI PlusIO system slot together with CompactPCI and / or CompactPCI Express and / or CompactPCI Serial peripheral boards.

2 Electrical Specifications

2.1 PCI Express®

CompactPCI PlusIO – PICMG 2.30 – permits to lead a total of four PCI Express® interfaces to the backplane. The Ultra Hard Metric connectors on the plug-in board permit data rates of up to 5 Gb/s, traditional 2-mm connectors being usable on the backplane.

The signals correspond to the following table:

PICMG 2.30 Mnemonic	[PCIe] Mnemonic	Description
PE_Rx00-	PERn0	Differential PCI Express Receiver Lane
PE_Rx00+	PERp0	
PE_Tx00-	PETn0	Differential PCI Express Transmitter Lane
PE_Tx00+	PETp0	
PE_CLK-	CREFCLKn	Differential 100 MHz Reference Clock
PE_CLK+	CREFCLKn	
PE_CLKE#	PRSNT1#	Presence Detect
	PRSNT2#	

Table 1. PCI Express® Signal Description

The number of the interface is added as a prefix followed by an underline to the signal name, e.g. 1_PE_Rx00-.

2.1.1 PCI Express® Configuration Possibilities with CompactPCI® PlusIO

The four PCI Express interfaces (also called links) can be used to control four PCI Express®-based peripheral boards. Each interface is equipped with one differential receive pair and a differential transmit pair – a lane. The four PCI Express® lines can e.g. be compatible to CompactPCI® Express or to CompactPCI® Serial.

Each interface reaches data rates of 250 MB/s with PCI Express® Gen1 or 500 MB/s with PCI Express® Gen2 per direction. For some applications, however, e.g. for image processing, these data rates are still not sufficient. For this reason, the PICMG Standard 2.30 CompactPCI PlusIO allows to "cluster" the four PCI Express® interfaces. This way, the four links with one lane each defined for PICMG 2.30 can also be configured as two links with two lanes each or even as one link with four lanes. In the last-mentioned case, theoretical data rates of 1000 MB/s with PCI Express® Gen1 or 2000 MB/s for Gen2 can be reached, but only with a connected device.

The PICMG 2.30 CPU board imports the configuration via four control lines which are also used to activate the respective 100 MHz clock which is allocated to a PCI Express® interface. No additional lines are necessary. This way, CompactPCI PlusIO PICMG 2.30 guarantees high flexibility for the connection of high-speed peripheral components based on PCI Express® while being 100% compatible to the established CompactPCI standard and without needing additional infrastructure like switches or bridges – a future-safe solution.

1_PE_CLKE#	2_PE_CLKE#	3_PE_CLKE#	4_PE_CLKE#	PCI Express Config.
open	open	open	open	Not defined
GND	open	open	open	1 link with 4 lanes
open	GND	open	open	2 links with 2 lanes
GND	GND	open	open	2 links with 2 lanes
open	open	GND	open	4 links with 1 lane
GND	open	GND	open	4 links with 1 lane
open	GND	GND	open	4 links with 1 lane
GND	GND	GND	open	4 links with 1 lane
open	open	open	GND	4 links with 1 lane
GND	open	open	GND	4 links with 1 lane
open	GND	open	GND	4 links with 1 lane
GND	GND	open	GND	4 links with 1 lane
open	open	GND	GND	4 links with 1 lane
GND	open	GND	GND	4 links with 1 lane
open	GND	GND	GND	4 links with 1 lane
GND	GND	GND	GND	4 links with 1 lane

Table 2. PCI Express® configuration

2.2 SATA/SAS

CompactPCI PlusIO – PICMG 2.30 – permits to lead a total of four SATA interfaces with data rates of 1.5 Gb/s or 3 Gb/s to the backplane. The signals correspond to the following table:

PICMG 2.30 Mnemonic	[SATA] Mnemonic	Description
SATA_Rx-	HR-	Host receiver signal pair
SATA_Rx+	HR+	
SATA_Tx-	HT-	Host transmitter signal pair
SATA_Tx+	HT+	

Table 3. SATA Signal Description

The number of the interface is added as a prefix followed by an underline to the signal name, e.g. 1_SATA_Rx-.

2.3 SGPIO

The CompactPCI PlusIO standard supports the following SGPIO signals:

PICMG 2.30 Mnemonic	[SFF] Mnemonic	Description
SATA_SC	Sclock	Clock signal (output)
SATA_SL	Sload	Last clock of a bit stream; begin a new bit stream on the next clock (output)
SATA_SDO	SDataOut	Serial data output bit stream (output)
SATA_SDI	SDataIn	Serial data input bit stream. SDataIn may not be supported by all SGPIO devices (input)

Table 4. SGPIO Signal Description

2.4 USB

The USB interfaces are compliant to the USB standard.

PICMG 2.30 Mnemonic	[USB] Mnemonic	Description
USB2-	D-	Differential Data Line
USB2+	D+	

Table 5. USB Signal Description

The number of the interface is added as a prefix followed by an underline to the signal name, e.g. 1_USB2-.

2.5 Ethernet

Ethernet is electrically compliant to 10BaseT, 100BaseT, 1000BaseT and 10GBaseT Ethernet.

These standards are based on copper based twisted pair connections. Such Ethernet connections can be used not just as a backplane interconnect but also to connect CompactPCI systems by cable. It is very common to support auto-negotiation on such Ethernet connections which guarantees best interoperability between different speed standards. The number of the interface is added as a prefix followed by an underline to the signal name, e.g. 1_ETH_A+.

PICMG 2.30 Mnemonic	[ETH] Mnemonic	RJ45 Pin #	Description
ETH_A+	TP0+	1	Differential Data Pair 0
ETH_A-	TP0-	2	
ETH_B+	TP1+	3	Differential Data Pair 1
ETH_B-	TP1-	6	
ETH_C+	TP2+	4	Differential Data Pair 2
ETH_C-	TP2-	5	
ETH_D+	TP3+	7	Differential Data Pair 3
ETH_D-	TP3-	8	

Table 6. Ethernet Signal Description

3 CompactPCI® PlusIO Interoperability Implementation Rules

To guarantee maximum compatibility between different board manufacturers and to optimize the usability in hybrid systems with CompactPCI Serial or CompactPCI Express the order to implement the interfaces is defined. Ethernet and USB are ascending; SATA/SAS is descending, PCI Express is alternating. If a system slot cannot support the maximum number of interfaces, the usability of peripheral slots is optimized.

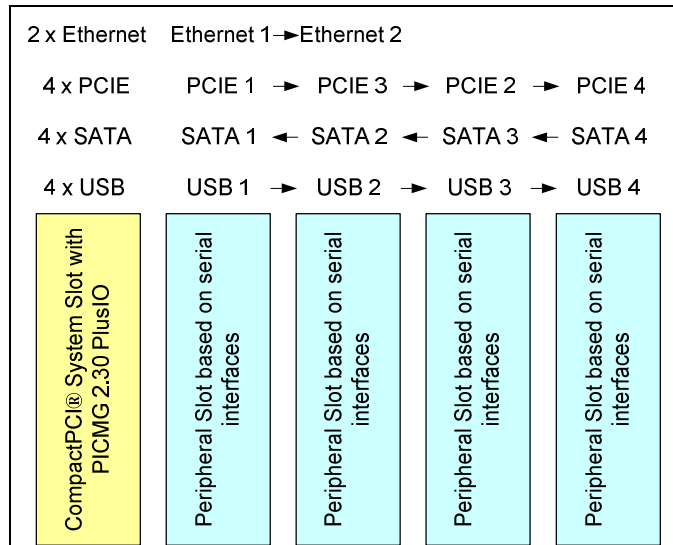


Figure 3. Example: All interfaces are implemented and connected to 4 peripheral boards

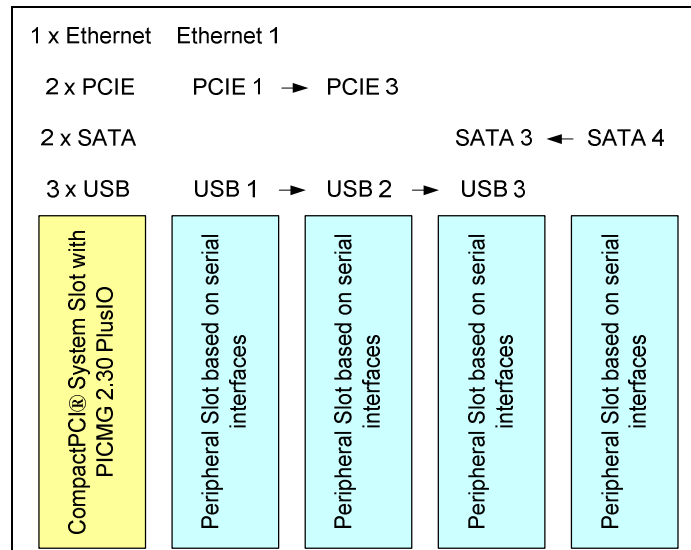


Figure 4. Example: Partial implementation of interfaces

3.1 Nomenclature for Interfaces

A board claiming to be compliant with standard 2.30 shows the supported interfaces in the following way in all technical data:

- <number of PCI interfaces>**PCI**<PCI Frequency>/
- <number of PCI Express Interfaces>**PCIE**<PCI Frequency Gb/s>/
- <number of SATA interfaces>**SATA/SAS**<SATA/SAS Frequency Gb/s>/
- <number of USB interfaces>**USB2**/
- <number of Ethernet Interfaces>**ETH**<Maximum Ethernet Frequency 10, 100, 1000, 1G or 10G>

A fully equipped board would be marked e.g. as: 1PCI33/4PCIE2.5/4SATA3/4USB2/2ETH1G whereas a board just supporting one Ethernet would be marked: 0PCI/0PCIE/0SATA/0USB2/1ETH1G.