

CompactPCI[®] Serial

Short Form Specification



Europe

**Open Modular
Computing Specifications**

NOTE: This short form specification is a subset of Revision 1.0 of the CompactPCI Serial specification PICMG CPCI-S.0, which is currently under development and can change. For complete guidelines on the design of CompactPCI Serial compliant boards and systems, the full specification is required.

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1 General

1.1 About CompactPCI Serial

The CompactPCI Serial specification defines a modular computer system, consisting of:

- A backplane
- A system slot
- Up to 24 peripheral boards.

CompactPCI Serial defines the support of PCI Express, SATA/SAS, USB and Ethernet, concurrently. PCI Express, SATA/SAS and USB are arranged as a simple star architecture. Ethernet is a full mesh. Switch boards are not required and therefore not described.

To support the high-speed serial interfaces a connector is introduced which is compatible to the IEEE1101 specification. The CompactPCI Serial specification supports data rates of up to 8 Gb/s for PCI Express, 6 Gb/s for SATA as well as USB 3.0 and 10 Gb Ethernet.

The mechanical design is fully backward compatible to CompactPCI and will interoperate with existing systems. This specification allows the implementation of hybrid backplanes: CompactPCI Serial with CompactPCI, CompactPCI PlusIO and/or with CompactPCI Express.

3U and 6U boards are supported with the main focus being on 3U. For 3U a new conductive cooling mechanical concept is introduced which allows to use all boards in a conductive cooled environment as well.

1.2 Migration from CompactPCI to CompactPCI Serial

CompactPCI is a well-established industrial specification for modular computers. The IEEE 1101 compliant mechanics are robust and proven in use. The electrical interface is based on the parallel PCI bus. This technology will successively be replaced by serial, high speed, point-to-point connections.

CompactPCI Serial uses the mechanical concept of CompactPCI and uses serial interconnect technology. CompactPCI Serial does not need special infrastructure hardware.

The migration from CompactPCI to CompactPCI Serial is made rather simple by using hybrid systems. Even for these, no dedicated switch or bridge boards are required because of specifications like PICMG 2.30.

PICMG 2.30 brings a limited number of serial interconnects to the backplane so that modern peripheral cards can be inserted into legacy CompactPCI systems. All mechanics are compatible to IEEE 1101.

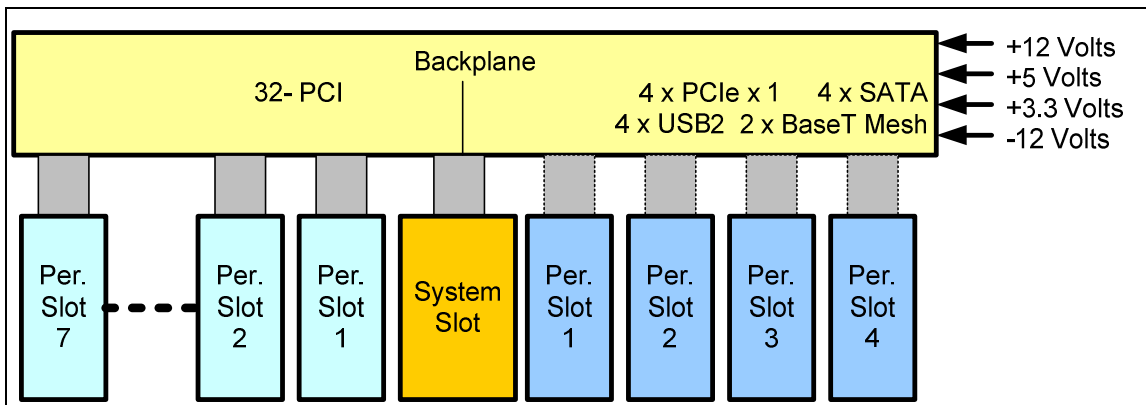


Figure 1. CompactPCI PlusIO Architecture

PICMG 2.30 CompactPCIPlusIO defines the usage of connector J2 in legacy CompactPCI systems in a way to bring some of the high speed serial interconnects to the backplane. A CompactPCI system slot which is compliant to PICMG 2.30 can control up to seven 32-bit legacy CompactPCI peripheral boards as well as up to four CompactPCI Serial peripheral boards with limited functionality.

This can easily be realized by means of a hybrid backplane carrying legacy boards as well as CompactPCI Serial boards because the two specifications, PICMG 2.0 and PICMG CPCI-S.0, are IEEE 1101 compliant.

1.3 CompactPCI Serial Architecture

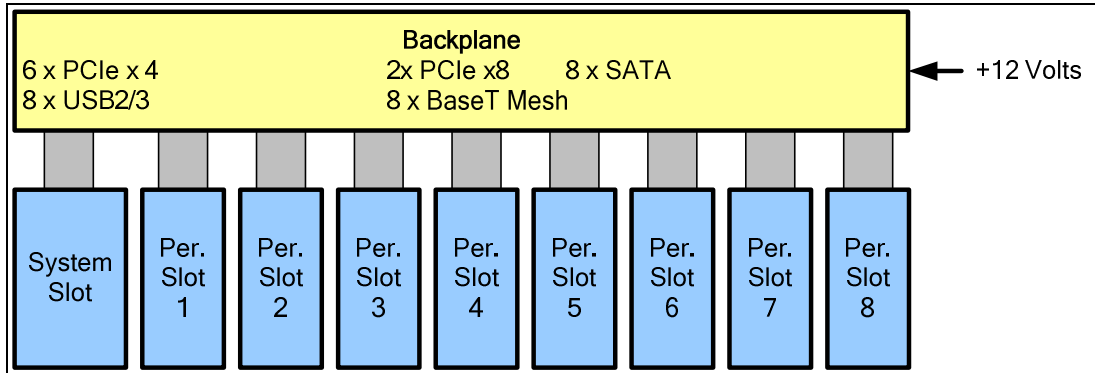


Figure 2. CompactPCI Serial Architecture

CompactPCI Serial uses all the mechanics of CompactPCI. The specification is compliant to IEEE 1101. Just the 2-mm hard metric connector is replaced by a more modern higher-density connector which is able to support differential signals of 10 Gb/s and even more. Like in CompactPCI the backplane is fully passive. Supply voltage within a 3U system is 12 Volts only and additional 48 Volts are supplied within a 6U system, which can be used for Power-Over-Ethernet applications.

Like in CompactPCI there is a dedicated system slot which provides the system with some minimal central infrastructure functions like reset and clock supply. This means that the smallest possible CompactPCI Serial system consists of just one single slot, the system slot.

Peripheral slots are connected by modern serial, high-speed, point-to-point connections as in MicroTCA, but requiring no switch or hub. Instead, a full star architecture is realized on the backplane for PCI Express, SATA and USB. For Ethernet a full mesh network is implemented on the backplane.

A system slot board can be used in a peripheral slot as well to do multiprocessing. The easiest way to communicate in this case is via Ethernet. Ethernet uses xxBase-T cable standards instead of dedicated backplane standards. This lowers the cost, guarantees better interoperability and offers currently up to 10 Gb/s data throughput.

Rear I/O is also supported like in CompactPCI systems but many more pins are available and higher speed is supported.

CompactPCI Serial uses the robust mechanics of CompactPCI, the modern serial interconnects but does not need dedicated infrastructure boards. CompactPCI Serial is designed for harsh environments and cost-critical applications demanding high throughput and reliability.

1.4 3U Mechanical Overview

A system based on CompactPCI Serial consists of the same components as a legacy CompactPCI system. Within this specification 3U systems as well as 6U systems are defined. A passive backplane is used to connect all front and rear boards. Every board is supplied with a front and rear panel. A handle (two handles for 6U) allows the user to plug-in and to remove a board from a rack. A maximum of six discrete connectors forms a slot and the amount of used connectors can vary depending on the application. Thereby maximum scalability and cost-effectiveness is achieved.

Figure 3 shows an example of a nine-slot 3U system. In this example the maximum amount of connectors on the backplane are assembled, to offer maximum connectivity.

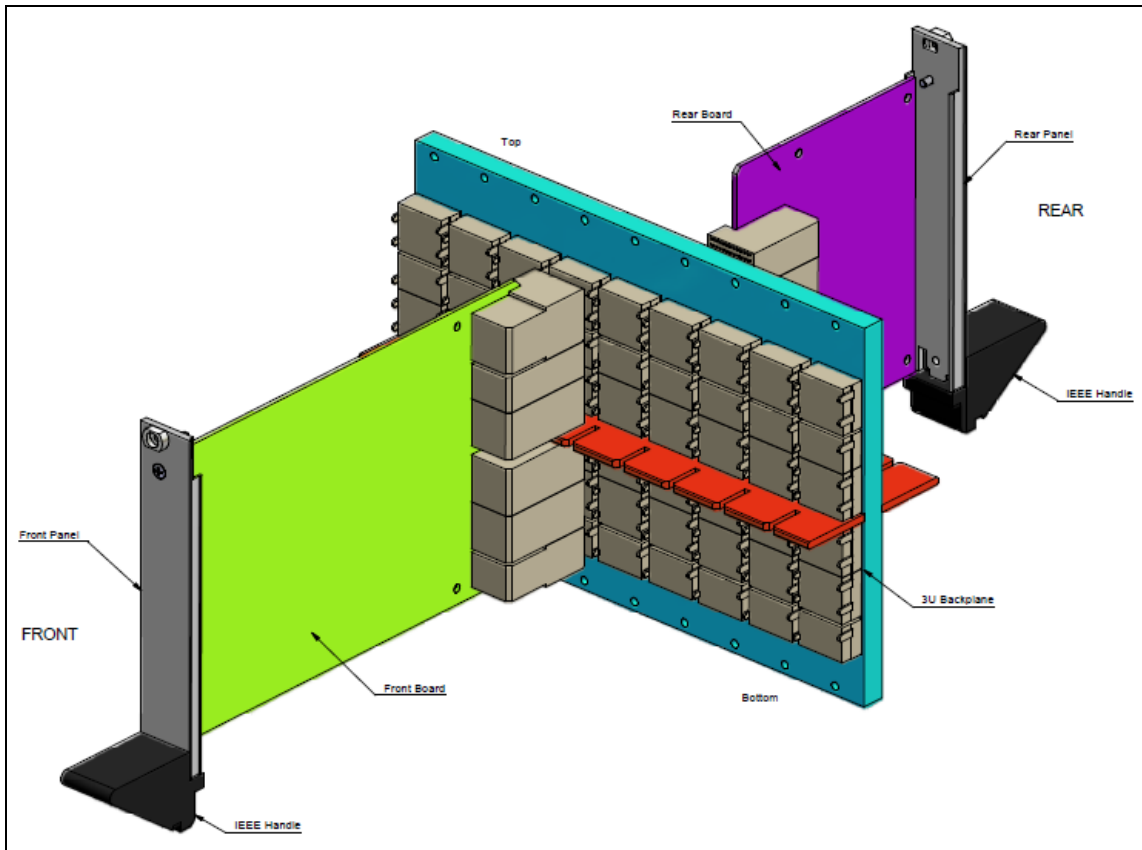


Figure 3. Mechanical Overview 3U Example

1.5 6U Mechanical Overview

Front and rear boards are defined for the 6U form factor. Compared to a 3U system one extra connector (J0/P0) is defined. This connector offers extra power (that will be needed in a 6U system) and also two further Ethernet connections, which can be used for system management (e.g. AMT). The backplane can be monolithic or split. Furthermore it is possible to define a user backplane which is a mixture of both (see Figure 4 and 5).

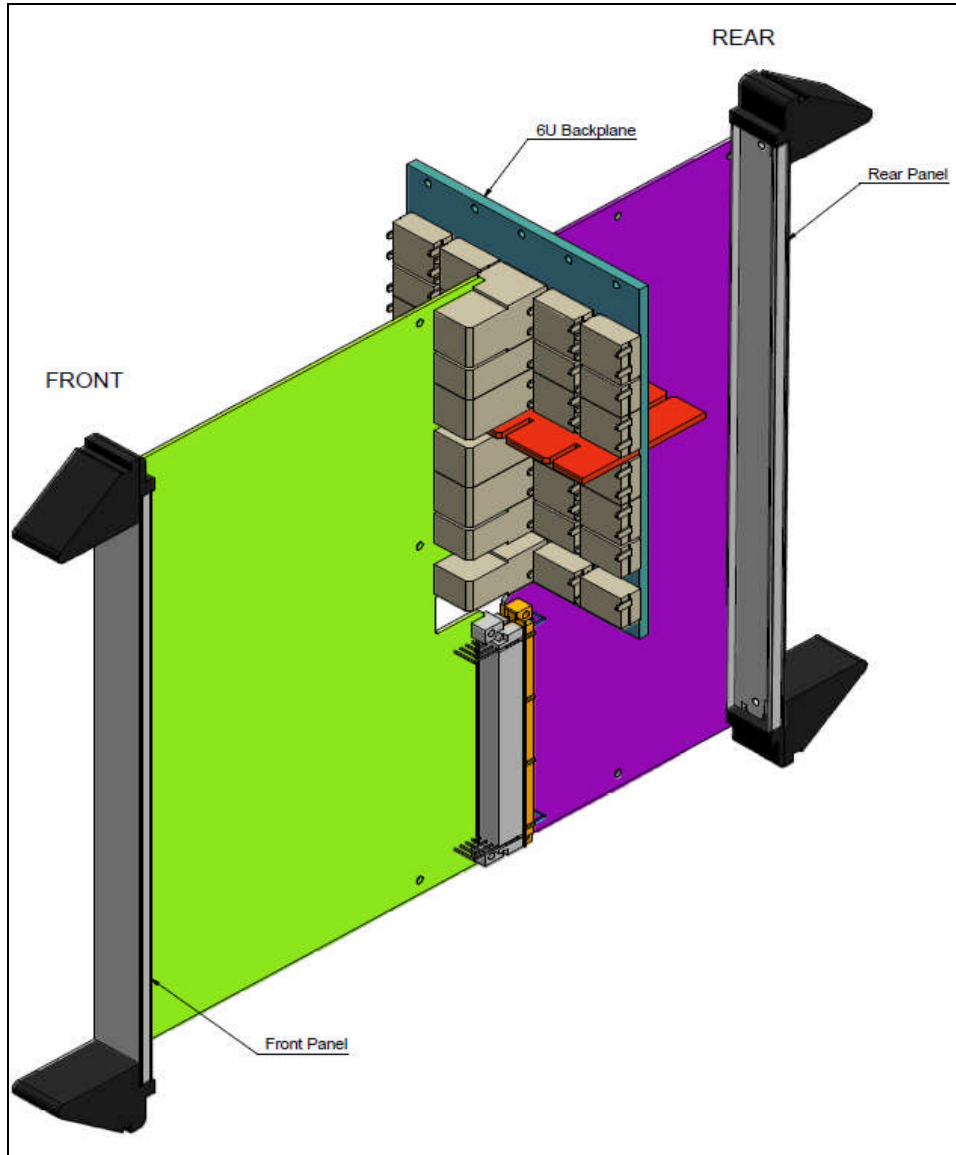


Figure 4. Mechanical Overview 6U Example (Split-Backplane / Front view)

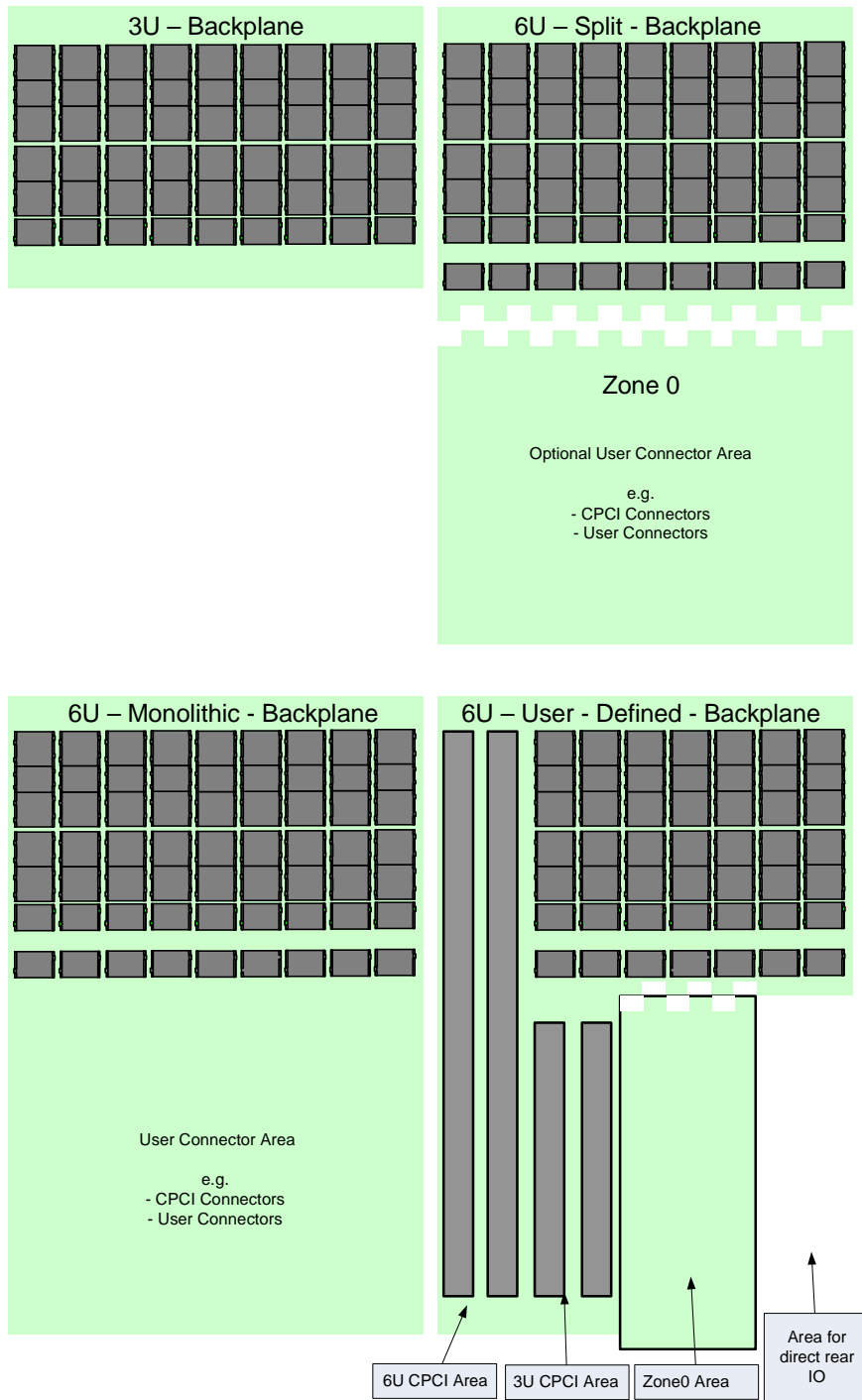


Figure 5. Backplane Example Drawings of 3U vs. 6U Variants

1.6 Connector Types

Connectors used for CompactPCI Serial are optimized for high-speed differential signal transmission. Shielding and impedance control is maintained through the connectors. The connector is arranged in rows with 12 pins each. 12 pins are sufficient for 4 high speed signal pairs. 4 pins in a row are required for ground. However the pins within the connector are not specialized. So a pin can be used for signals (differential or single ended), for ground, as well as for the supply voltage.

For front boards receptacle connectors are used on the backplane, and right angle headers are used on the plug-in boards. On rear boards it is vice-versa. All connector types are designed for press-fit mounting. The press-in pin length in the PCB is just 1.6 mm to minimize the stub lengths thereby enhancing the signal integrity. To realize rear I/O, a plug connector is pressed on to the back of the backplane. This mirrors the pin assignment from the front to the back side.

To connect the front boards to the backplane, four different plug types of the same connector family are used.

Designator	Type	Number of Rows	Number of Walls	Usage
P0	A	6	4	Optional
P1	A	6	4	Mandatory
P2	B	8	2	Optional
P3	B	8	2	Optional
P4	B	8	2	Optional
P5	C	6	2	Optional
P6	D	8	4	Optional

Table 1. Front Board Connector Types

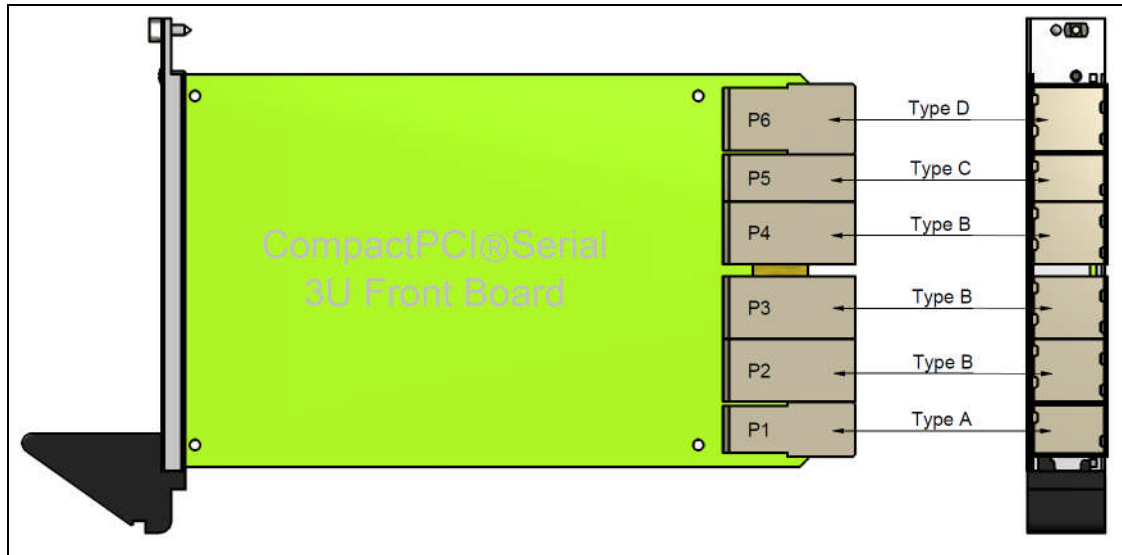


Figure 6. 3U Connector Plug Types A, B, C and D on Front Boards

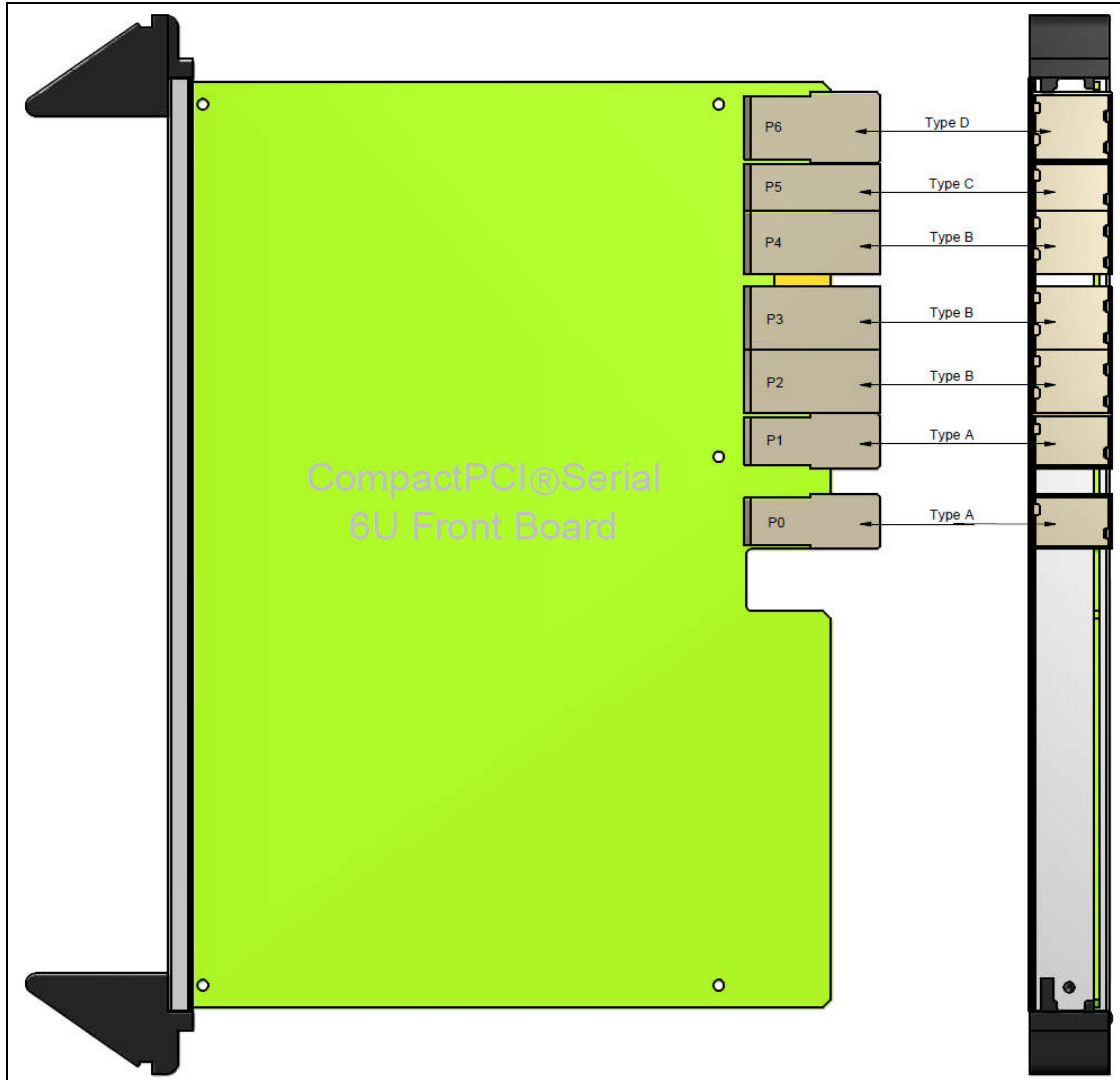


Figure 7. 6U Connector Plug Types A, B, C and D on Front Boards

On the backplane there are just 2 different types of receptacles, type E – a six row version and type F – an eight row version. The six row receptacle connects to all type A as well as to type C plugs. The eight row receptacle connects to all type B as well as to type D plugs.

Designator	Type	Number of Rows	Usage
J0	E	6	Optional
J1	E	6	Mandatory
J2	F	8	Optional
J3	F	8	Optional
J4	F	8	Optional
J5	E	6	Optional
J6	F	8	Optional

Table 2. Backplane Connector Types

1.7 Rear Board Connector Types and Reference Designation

To connect the rear boards to the backplane, two different receptacle types of the same connector family are used.

Designator	Type	Number of Rows	Number of Walls	Usage
rJ2	H	6	2	Optional
rJ3	G	8	2	Optional
rJ4	G	8	2	Optional
rJ5	H	6	2	Optional

Table 3. Rear Board Connector Types

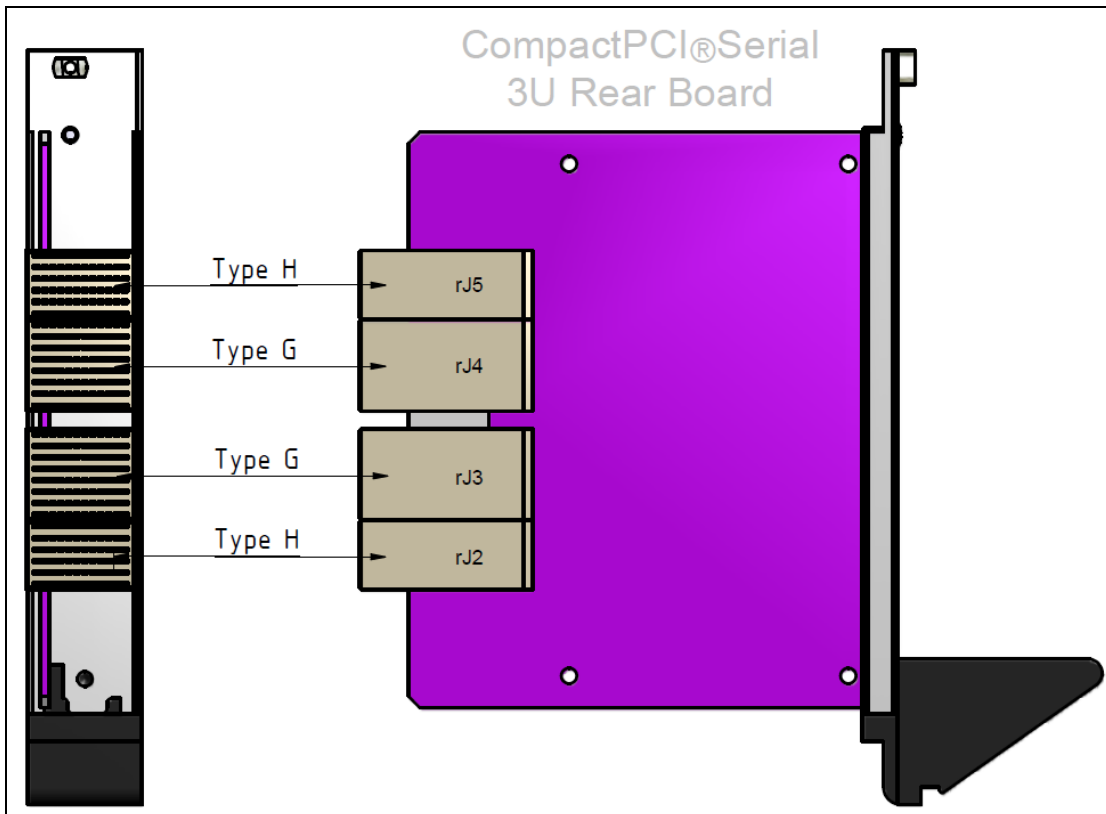


Figure 8. Connector Plug Types H and G on Rear Boards

Designator	Type	Number of Rows	Usage
rP2	J	6	Optional
rP3	I	8	Optional
rP4	I	8	Optional
rP5	J	6	Optional

Table 4. Rear Backplane Connector Types

1.8 ESD Protection

A CompactPCI Serial system is equipped with an ESD strip and an ESD clip. When a board is inserted into an enclosure, the ESD strip connects with an ESD clip on the card guide which is connected to chassis ground. The ESD strip is separated into three segments to achieve a “controlled discharge”. The first segment is connected to the front panel through a 10 MOhm resistor to discharge any built-up static charge from the board or user. The resistor is used to limit the amount of discharge current. The second segment discharges the board’s ground planes as it is inserted further into the card guide; again through a 10 MOhm resistance. The final third segment has a direct connection to the front panel. This provides a discharge path as the backplane connectors engage and when the board comes to rest after being completely installed. The third segment also provides a discharge path from the front panel to chassis ground when the entire system is assembled making it safe for handling and operation. The ESD card guide clip contacts the board edge as the board is inserted in the system and provides a path for ESD energy on the board to be discharged into the chassis.

1.9 Mezzanine Board

Implementation of the Ethernet connection of a system board can be done with a mezzanine board. Due to this concept more flexibility will be achieved, because the usage of Ethernet does not depend on the system board itself. Furthermore different mezzanine boards can offer a different number of Ethernet connections, thereby obtaining maximum scalability. If this concept is implemented, the CompactPCI Serial system board becomes a mezzanine host and the mezzanine board can be plugged onto this host. The connector P6 is then placed on the mezzanine board and a cut-out on the mezzanine host is provided. Only the interconnection between the mezzanine host to the CompactPCI Serial backplane will be specified within this specification. As shown in figure Figure 9 and Figure 10 the mezzanine concept can be implemented within a 3U and a 6U system.

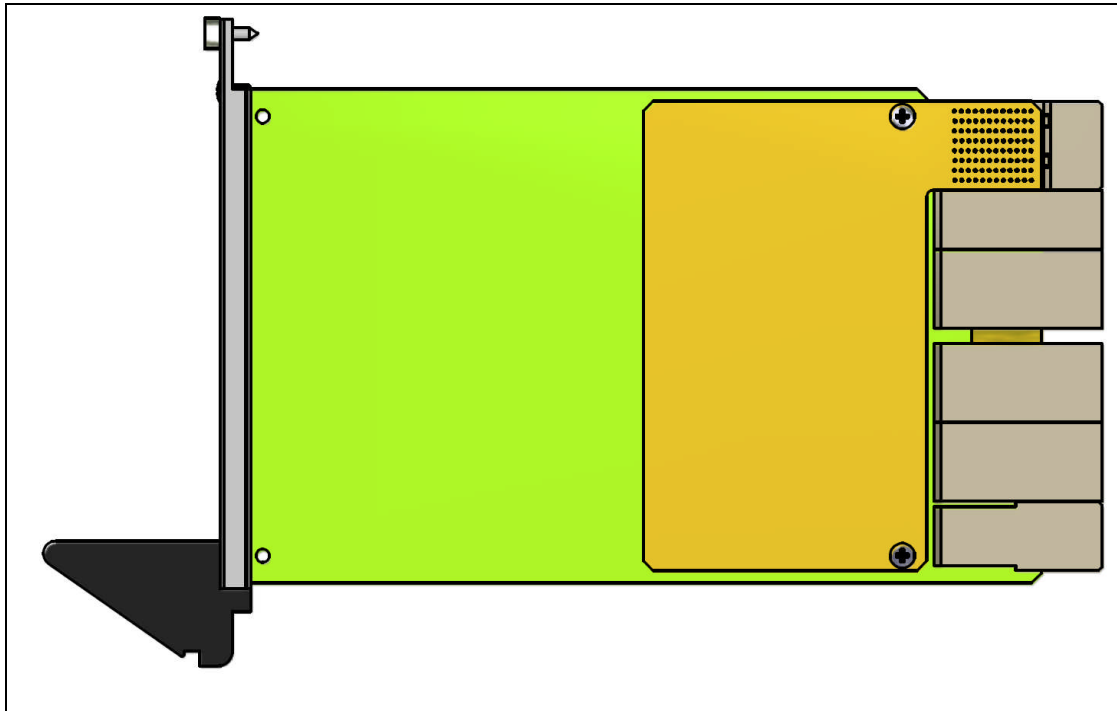


Figure 9. 3U Mezzanine Concept

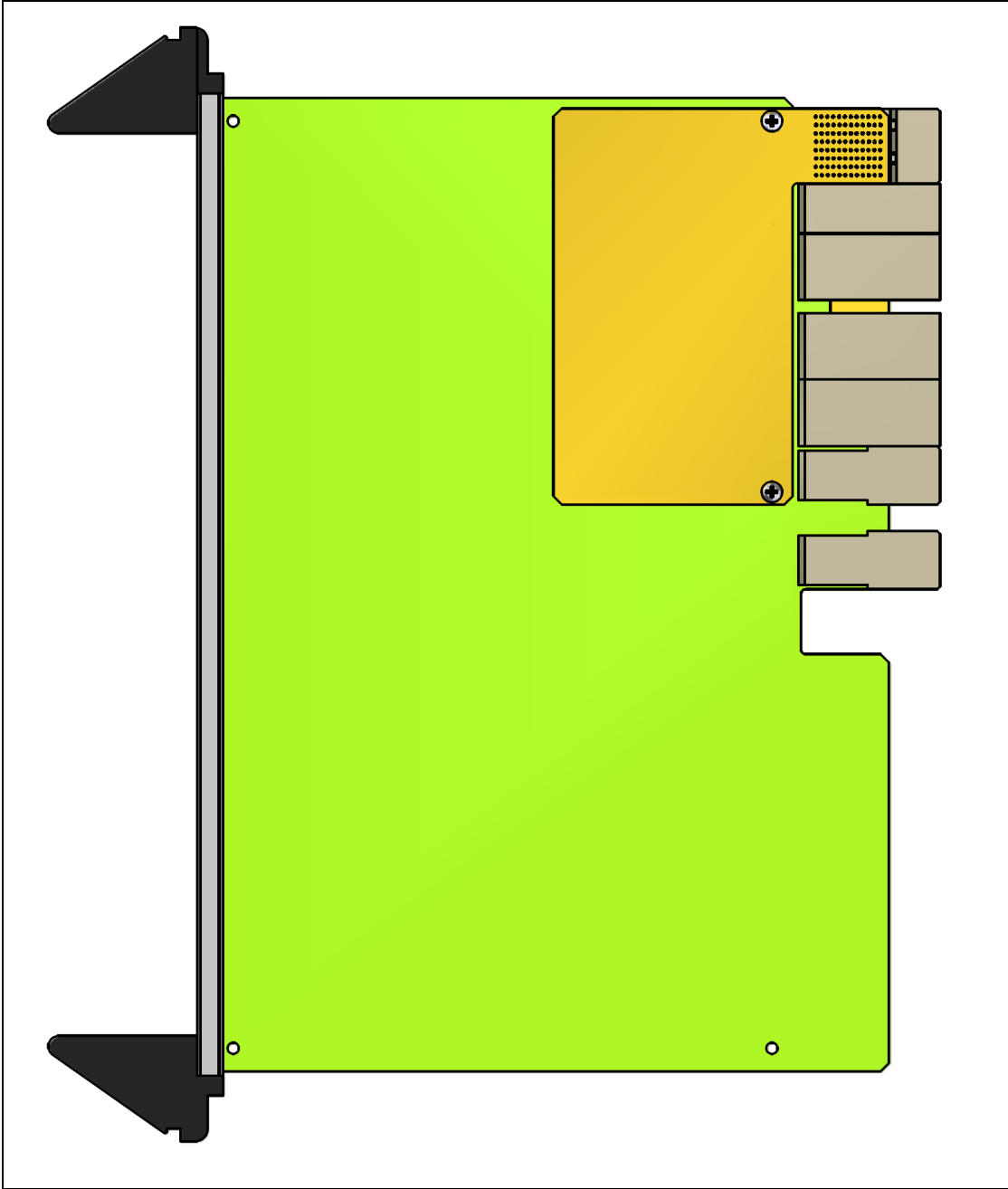


Figure 10. 6U Mezzanine Concept

1.10 Compatibility Glyphs

As defined in the standard, system slots and peripheral slots are clearly marked by glyphs.



Figure 11. Compatibility Glyphs Examples

1.11 Backplane Guide Element

To guarantee best fitting of the board connectors into the backplane connectors, and also if a board is plugged in harsh environments, a guide on the backplane is defined. One guide element within a 3U/6U system and an extra guidance rail within a 6U system is required. If no guide is used (especially within a 6U system), there is a potential for damage to the connectors if there is board warp or if the boards are not carefully aligned during plugging. Furthermore the board needs to be centered within the “default” guide rail (card guide) that fits the board within a rack.

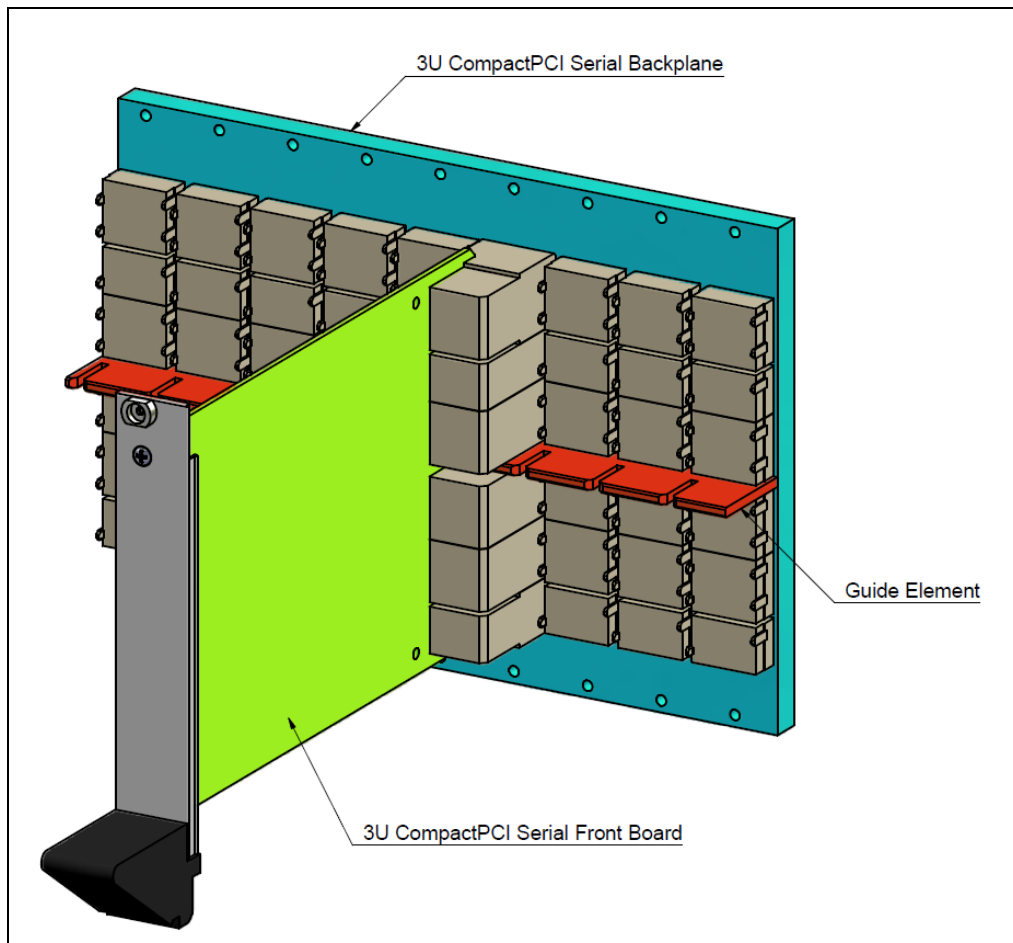


Figure 12. Guide Element Overview

Conductive Cooled Assembly

The CompactPCI Serial also defines an enclosure and a cassette for conduction cooling. Conductive cooled boards need 5HP space in a system.

2 Electrical Requirements

2.1 Backplane Power Distribution

CompactPCI Serial relies on a single rail +12V main power supply. +5V standby is optionally available. -48V optional voltage is available within a 6U system only. The backplane distributes the supply voltages to the front boards. Rear boards are indirectly supplied by the corresponding front board.

2.2 Power Control

The power control signals PS_ON#, PWRBTN#, PWR_FAIL# are routed from the system slot to a utility connector.

PS_ON# allows a system board to remotely control the power supply in conjunction with features such as soft on/off, Wake on LAN, or wake-on-modem.

The PWRBTN# signal may be used to control the power supply's PS_ON# signal. Furthermore it could be used to shut down the operating system etc.

Power supplies providing the PWR_FAIL# signal show that the output voltage will leave the rated output value in short time. System boards can use this information to shut down the system in a defined way. This specification does not define details about this behavior.

2.3 Platform Control Signals

2.3.1 Reset Signals

The PRST# signal of the system slot is routed to a utility connector. The RST# output signal of the system slot is routed to all RST# input signals of the peripheral slots.

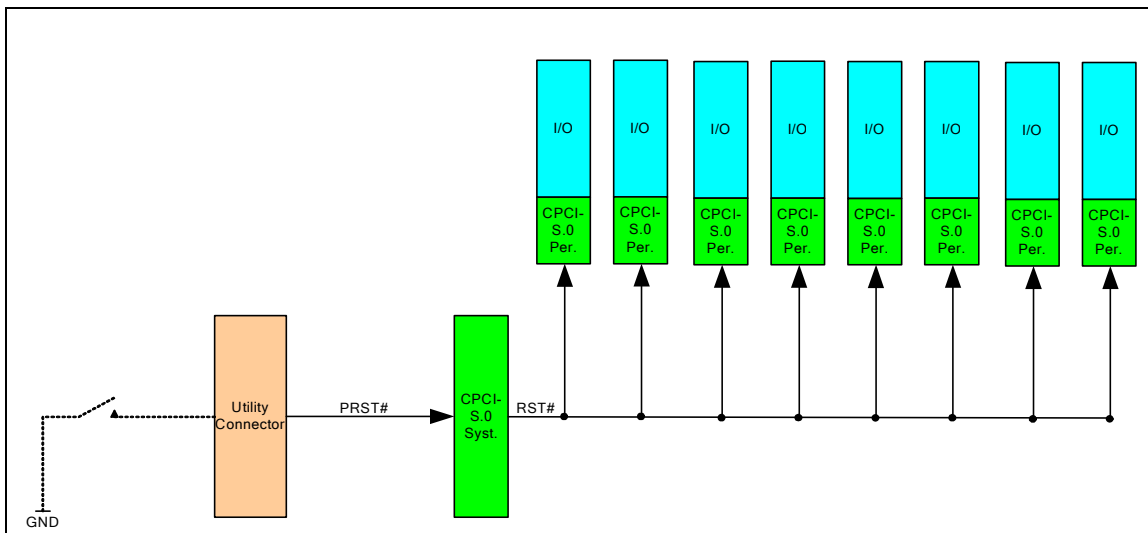
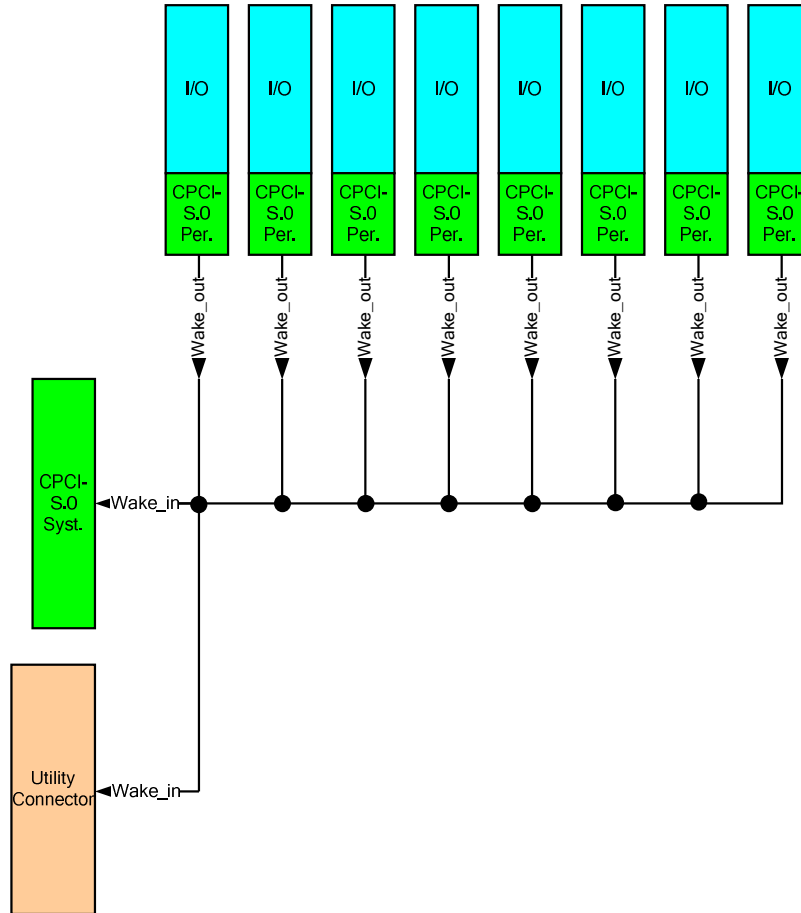


Figure 13. Backplane Routing Reset

2.3.2 Wake

The WAKE_IN# signal of the system slot is routed to all WAKE_OUT# signals of the peripheral slots.

Figure 14. Backplane Routing Wake



2.3.3 System Slot Detection

Every slot at the backplane provides a System Slot Identification pin (SYSEN#). The SYSEN# pin is connected to GND at the system slot and left open on peripheral slots. Boards capable of system slot support detect SYSEN# low to activate system slot functionality e.g. RST#, PS_ON# etc.

2.3.4 Geographical Addressing

Due to the fact that within CPCI-S.0 each physical SATA port always needs the same geographic address (because of SGPIO), geographical addresses do not follow the physical slot numbers, but the SATA filling order.

Backplanes support the GA[3:0] geographic addressing signals for unique slot identification.

The highest slot number within a CPCI-S.0 system has geographic address 0. The next lower slot number has geographic address 1 up to the first peripheral slot.

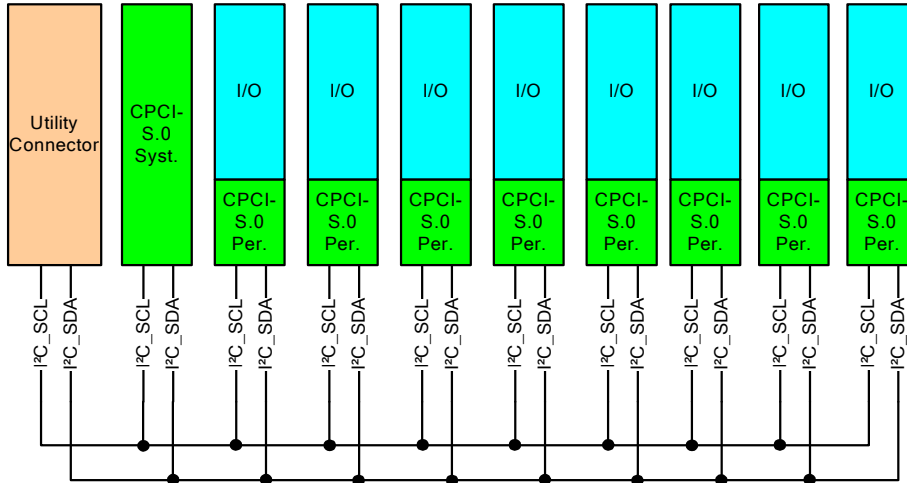
Peripheral boards can use geographical addressing based on GA[0], GA[1] and GA[2]. GA[3] can be used for systems with more than 8 peripheral slots.

2.4 Management Interfaces

2.4.1 I²C System Management Bus

The I²C System Management Bus is electrically compliant to the SMBus specification. The System Management Bus I²C_SCL and Bus I²C_SDA signals are bussed to every slot and the utility connector.

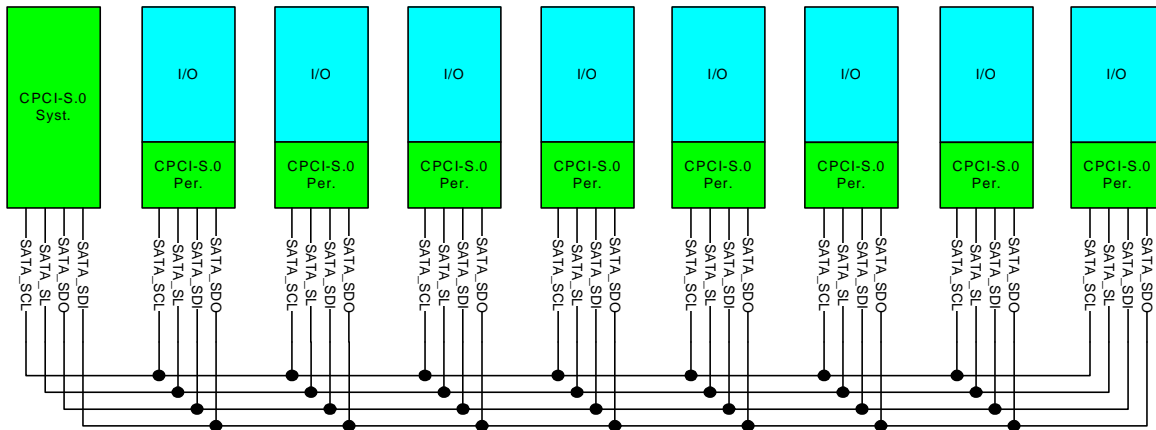
Figure 15. System Management Bus Signal Routing



2.4.2 Serial GPIO

The SATA_SCL, SATA_SL, SATA_SDO, and SATA_SDI signals from the system slot are bussed to the respective signals on the peripheral slots.

Figure 16. Serial GPIO Signals Backplane Routing



2.5 Precedence Order Rules to Implement Interfaces (Filling Order)

To guarantee maximum compatibility between different board manufacturers and to optimize the usability in systems with CPCI-S.0 the order to implement the interfaces is defined. PCIe, Ethernet and USB are ascending; SATA/SAS is descending. In case a system slot does not support the maximum number of interfaces, the usability of peripheral slots is optimized.

Figure 17. Precedence Order Rules to Implement Interfaces (Filling Order)

