



Europe

**Open Modular
Computing Specifications**

CompactPCI Express – the logical next step

Introduction PCI Express

In general there is a move from parallel busses to serial busses, especially with Ethernet and USB. Serial busses support hot-swap better, and provide a higher scalability in processor-to-processor and system-to-system architectures. Moreover, it uses less hardware estate and less connector size.

The definition of PCI Express is a scalable full-simplex serial bus standard that operates at 2.5 Gbps and offers both asynchronous and isochronous data transfers (where isochronous deals with data associated with time-sensitive applications, such as audio or video applications).

One can look at PCI Express as being the transformation of the parallel PCI bus to a serial, packet based bus. PCI Express is targeted for chip-to-chip, board-to-board, and box-to-box connections, and is developed under the control of PCI-SIG – Special Interest Group. Being backwards compatible, concerning the software it allows the application and driver developer to use the same software tools used to develop PCI-based software. This provides PCI Express with a unique feature: it does not need a protocol conversion while acting both as host bus and as expansion bus. This gives it an unmatched level of performance scalability.

CompactPCI Express overview

CompactPCI Express is a PICMG standard with the base standard called PICMG EXP.0, which was released in 2005. The move from CompactPCI to CompactPCI Express includes the influence from the Telecom Equipment Manufacturers with high availability architectures up to 99.999%, which need additional items like hot swap and system management.

Base features of CompactPCI, such as user I/O pins, rear transition I/O modules, support for additional busses like Computer Telephony, and base mechanicals

remain in the CompactPCI Express standard. In practice this means for a 6U CompactPCI Express module the J3-J5 mechanical attributes are the same as the base CompactPCI standard.

The difference lies in the J1 and J2 connectors of CompactPCI, which are replaced with improved connectors. The power supply is via a 7-pin Universal Power Module, UPM, capable of delivering over 400W of power to individual modules. The high speed PCI Express interconnect is achieved with a 3-row Advanced Differential Fabric connector. Two of these connectors are used, providing up to 120 Gbps bandwidth to the backplane.

A mini, enriched 2 mm hard metric connector functions in several capacities depending on the slot in which it is used. It is a keyed connector that can provide rear I/O for 3U modules, provide power to low-power modules (<34W), PXI trigger signals, or geographical addressing.

To leverage the wide array of available 3U and 6U CompactPCI modules, hybrid designs of CompactPCI / CompactPCI Express backplanes are becoming available. With these, a smoother transition is possible.

Serial Communication on CompactPCI Express via lanes

The implementation of the PCI express bus consists of a bi-directional bus, effectively doubling the capacity versus parallel busses. For this two differential pairs are combined in so called “lanes” – one for each direction. A lane is a set of differential signal pairs, one pair for transmission and one pair for reception. A by-N Link is composed of N Lanes.

With this, options are possible, like:

by-1, x1 - A Link or Port with one Physical Lane.

by-4, x4 - A Link or Port with four Physical Lanes.

by-8, x8 - A Link or Port with eight Physical Lanes.

by-N, xN - A Link with “N” Physical Lanes.

CompactPCI-Express supports up to 16 of these lanes, so 16 bi-directional high speed communication lanes, totaling to 4GBytes/s each way, which is about 30 times faster than CompactPCI, and faster than a 10Gbits/s Ethernet link.

CompactPCI-Express supports point-to-point connections over these lanes, meaning that there are direct connections within a system via the backplane.

Boards and Slots – the basics to connect

This specification defines different slot and board types to meet the needs of different market segments, as well as ease the transition and speed of the adoption of this standard. The slot types defined include:

System Slot - the slot in a CompactPCI Express Chassis that accepts a System Board. The System Slot is Physical Slot 1. It provides up to four high-bandwidth PCI Express Links, Rear I/O, and power to support current and future processor requirements.

Type 1 Peripheral Slot - A slot with up to two PCI Express Links routed to it that accepts either a Type 1 or Type 2 Peripheral Board. It is similar to the System Slot definition, allowing System Boards to operate in Peripheral Slots.

Type 2 Peripheral Slot- A slot with one high-bandwidth PCI Express Link routed to it and Rear I/O. It accepts a Type 2 Peripheral Board.

Hybrid Peripheral Slot - supports either a Type 2 Peripheral Board, a 32-bit CompactPCI Board, or a PXI Board with the eHM connector populated instead of the J2 connector and a Switch Slot.

The board types that match these slots include:

System Board - provides the PCI Express Root Complex in the CompactPCI Express System, and it provides the power supply control signaling, reset, and System Management Bus master functionality

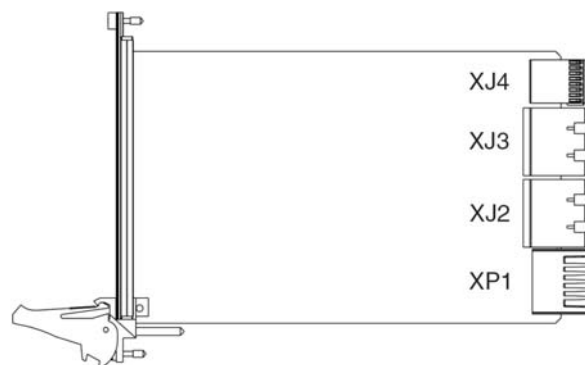
Type 1 Peripheral Board - A board designed to work in a Type 1 Peripheral Slot.

Type 2 Peripheral Board- A board designed to work in a Type 2 Peripheral Slot as well as Type 1 Peripheral Slot and Hybrid Peripheral Slot and a Switch Board.

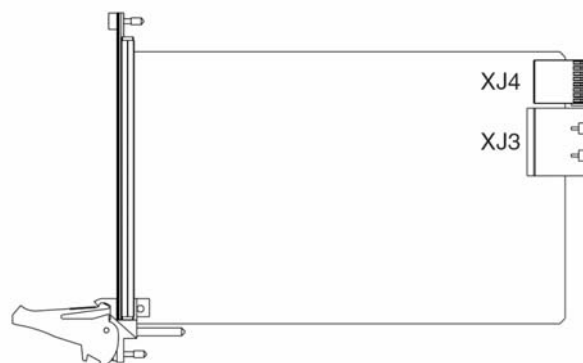
For backward compatibility with CompactPCI, several combinations are defined. Overall they are referred to as **Legacy Slot** and **Legacy Board** - refers to slots or Peripheral Boards defined in the PICMG 2.0 (CompactPCI) specification. These different board and slot types in the 6U form factor may include any or all of the J3/P3, J4/P4, and J5/P5 connectors defined in the PICMG 2.0 (CompactPCI) specification.

Let us take a closer look at some of the types. For simplicity, the pictures are only shown in the 3U format, but have similar 6U constructs. For details, please refer to the standard itself.

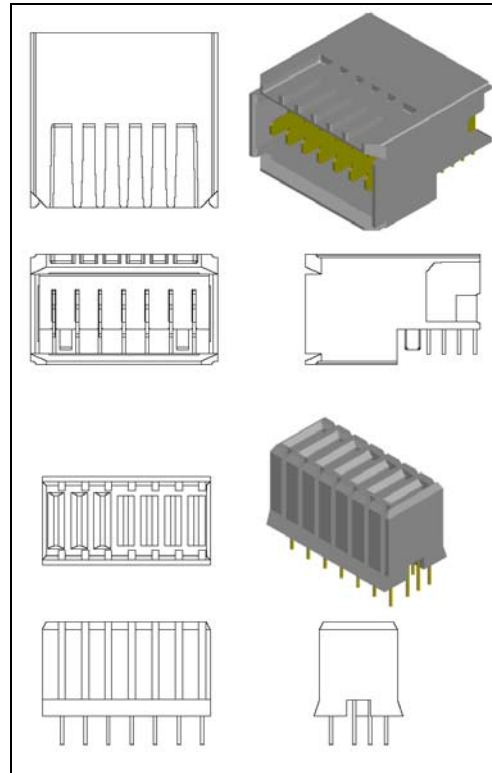
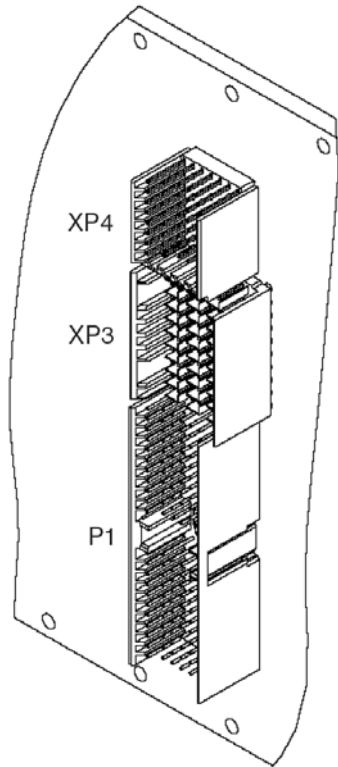
A **System Board** provides two or four PCI Express Links that lead to the PCI Express Root Complex, along with their associated PCI Express reference clocks. It also provides the power supply control signaling, reset, and optionally SMBus master functionality. A System Board can be designed to work as a Type 1 Peripheral Board also. The System Board connectors include the XP1 7-position power connector, the XJ2 ADF connector, the XJ3 ADF connector, and the XJ4 eHM connector. The figure below shows a System Board.



A **Type 2 Peripheral Board** has access to one PCI Express Link. The Type 2 Peripheral Board connectors include the XJ3 ADF connector and XJ4 eHM connector. See hereunder.



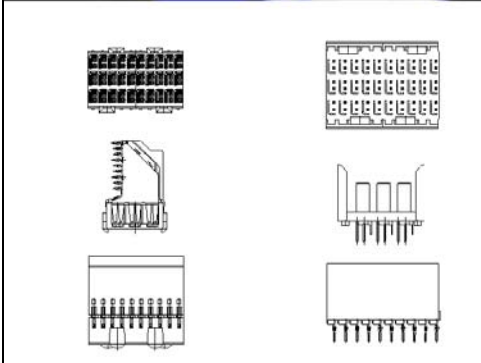
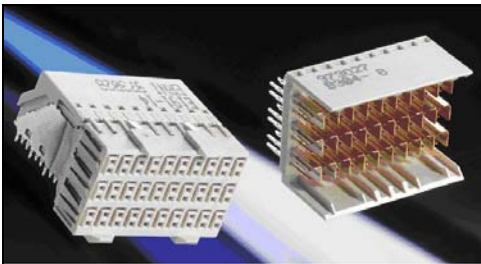
A **Hybrid Peripheral Slot** supports a Type 2 Peripheral Board, a 32-bit CompactPCI Board, or a PXI Board with an eHM connector populated instead of the J2 connector. This allows a single slot to work with new or existing products. The Hybrid Peripheral Slot connectors include the P1 connector defined in the PICMG 2.0 (Compact PCI) specification, the XP3 ADF connector, and the XP4 eHM connector.



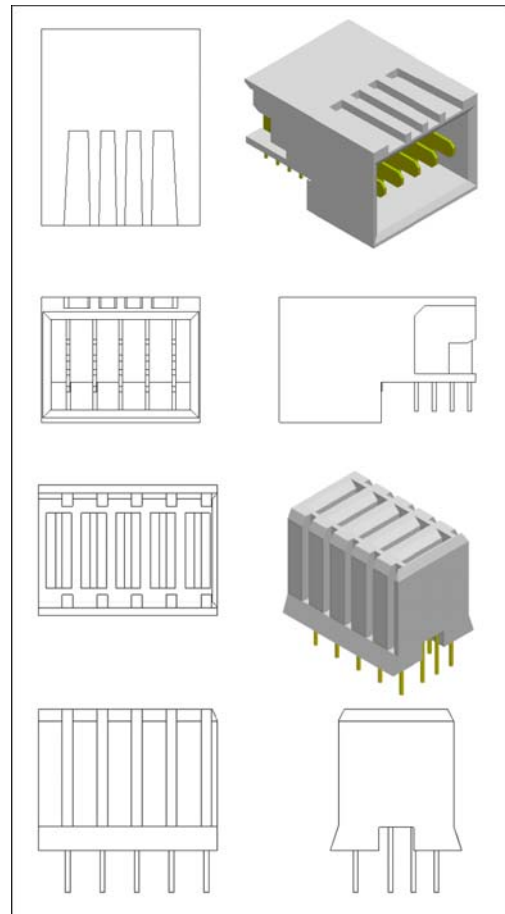
UPM Power Connector for System and Type 1 Peripheral Slots/Boards

Connectors – making the connection between the modules and the backplane

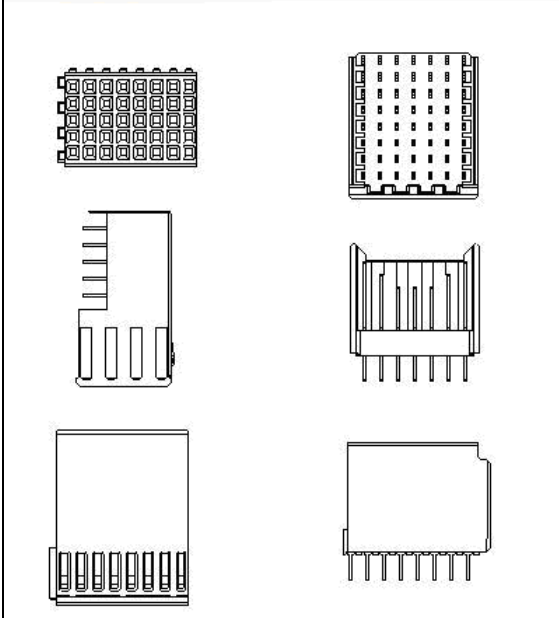
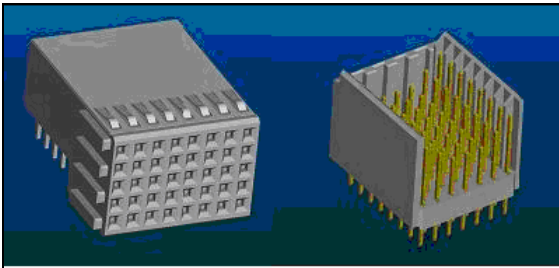
The CompactPCI Express specification uses legacy CompactPCI connectors, new high-speed connectors, a new power connector, and a new HM connector called an eHM connector to define several different slot and board types.



High-Speed Advanced Differential Fabric Connectors

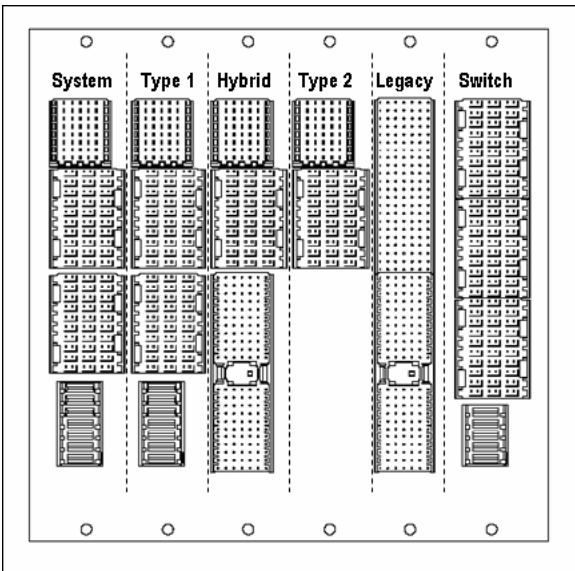


Power Connector for Switch Slots/Boards



eHM connector (5-row by 8-column Hard Metric connector)

CompactPCI Express 3U slot examples



System and Platform Management

For stand alone applications, and higher up-time, the management functions are integrated in the specification. System management is now supported via software control of the system. Remote diagnostics extends the usability of the technology.

Platform management is done via the IPMI - Intelligent Platform Management Interface, as defined in the Intelligent Platform Management Interface Specification. It provides a specification and mechanism for inventory management, monitoring, logging, and control for elements of a computer system.

What is PICMG Europe?

PICMG Europe is the neutral promoter of the PICMG technologies in Europe. The definition of the technical specifications is managed by the parent organization in the United States. The European branch office, PICMG Europe, was established in 1997.

The writing of the specifications is one aspect.

Marketing of the technology and products is the necessary next step. PICMG Europe is a dedicated, independent association for supporting this goal.

By marketing these technical specifications as a group, we are stronger than a number of individually operating companies. Moreover, users expect from open environments that products from different manufacturers are compatible on the same back panel. PICMG Europe is supported by its members, as well as it supports its members. For instance, every member receives all specifications, updates and changes, free of charge. With this they are sure they are using the latest versions only. Membership levels include suppliers, users and system integrators. As such, PICMG Europe is an organization to join if you are active in these markets.

For more information please check www.picmgeu.org